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Implementation of low power CMOS design using Adiabatic Improved Efficient Charge Recovery Logic

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Abstract* : *This paper presents a new adiabatic circuit technique called Positive Feedback Adiabatic Logic (PFAL). Power reduction is achieved by recovering the energy in the recovery phase of the supply clock. Energy dissipation comparison with other logic circuits is performed. The main objective of this paper is to provide new low power solutions for Very Large Scale Integration (VLSI) designers. The dynamic power requirement of CMOS circuits is rapidly becoming a major concern in the design of personal information systems and large computers. The adiabatic logic structure dramatically reduces the power dissipation. The adiabatic switching technique can achieve very low power dissipation, but at the expense of circuit complexity. Adiabatic logic offers a way to reuse the energy stored in the load capacitors rather than the traditional way of discharging the load capacitors to the ground and wasting this energy.

Keywords---Static CMOS, adiabatic algo, ECRL, PFAL, micro wind tool etc.

I. Introduction

Energy efficiency has become a major design concern in high-performance and mobile computer systems. Excessive power dissipation requires increasingly large, heavy, expensive, and noisy cooling machinery including special packages, heat sinks, heat pipes, and fans. Excessive energy consumption on mobile computer systems results in increasingly large, heavy, and expensive batteries, power conversion circuits, or fuel-cells, which themselves may introduce further heat removal issues. Several effective power management design techniques have been developed over the past few years, including lowering the supply voltage. As process scaling continues below 90nm, however, it becomes more difficult to scale the supply voltage for several reasons. The Energy dissipation in conventional CMOS circuits can be minimized through adiabatic technique. By adiabatic technique dissipation in PMOS network can be minimized and some of energy stored at load capacitance can be recycled instead of dissipated as heat. But the adiabatic technique is highly dependent on parameter variation. With the help of micro wind layout simulator, the energy consumption is analyzed by variation of parameter. In analysis, two logic families, ECRL (Efficient Charge Recovery Logic) and PFAL (Positive Feedback Adiabatic Logic) are compared with conventional CMOS logic for inverter circuits. It is finding that adiabatic technique is good choice for low power application in specified frequency range.

II. Principle of adiabatic switching

The word *ADIABATIC* comes from a Greek word that is used to describe thermodynamic processes that exchange no Energy with the environment and therefore, no energy Loss in the form of dissipated Heat. The fundamental of adiabatic switching can be interpreted with the inverter structure shown in Fig. 1 In conventional level-restoring CMOS logic circuits with rail-to-rail output voltage swing, each switching event causes an energy transfer from the power supply to the output node or from the output node to the ground. During a 0-to-*VDD* transition of the output, the total output charge $Q = Cload\ VDD$ is drawn from the power supply at a constant voltage. Thus, an energy of $Esupply = Cload\ VDD^2$ is drawn from the power supply during this transition. Charging the output node capacitance to the voltage level *VDD* means that at the end of the transition, the amount of stored energy in the output node is $Stored = Cload\ VDD^2 / 2$. Thus, half of the injected energy from the power supply is dissipated in the PMOS network while only one half is delivered to the output node. During a subsequent *VDD* -to- 0 transition of the output node, no charge is drawn from the power supply and the energy stored in the load capacitance is dissipated in the NMOS network. To reduce the dissipation, the circuit designer can minimize the switching events, decrease the node capacitance, reduce the voltage swing, or apply a combination of these methods. Yet in all these cases, the energy drawn from the power supply is *used* only once before being dissipated. To increase the energy efficiency of the logic circuits, other measures can be introduced for recycling the energy drawn from the power supply. A novel class of logic circuits called *adiabatic logic* offers the possibility of further reducing the energy dissipated during the switching events, and the possibility of recycling, or reusing, some of the energy drawn from the power supply. To accomplish this goal, the circuit topology and the operation principles have to be modified, sometimes drastically. The amount of energy recycling achievable using adiabatic techniques is also determined by the fabrication technology, switching speed, and the voltage swing. However, one can achieve very low energy dissipation by slowing down the speed of operation and only switching transistors under certain conditions. The signal energies stored in the circuit capacitances are recycled instead, of being dissipated as heat. The adiabatic logic is also known as *ENERGY RECOVERY CMOS*.

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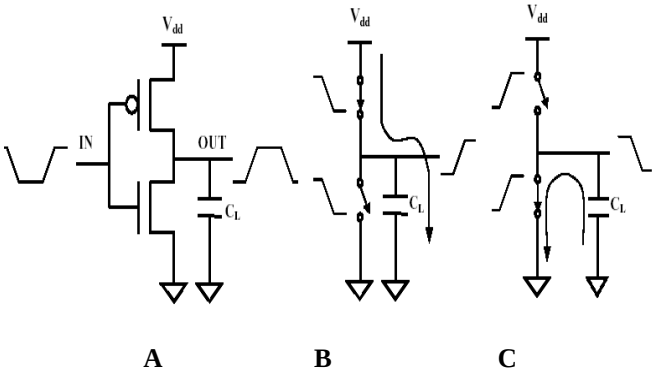

Fig1 Inverter Circuit explaining Adiabatic Switching.

The voltage across the switch = IR

P (t) in the switch = I^2R

Energy during charge = I^2RT

Hence

$E = I^2 RT = (CV/T)^2 RT = C^2V^2R/T$

$= (RC/T)\ CV^2 = (2RC/T)\ (CV^2)/2$

Where, the various terms of above equation are described as follows:

E — energy dissipated during charging,
Q — charge being transferred to the load,
C — value of the load capacitance,
R — resistance of the MOS switch turned on,
V — final value of the voltage at the load,
T — time spent for charging.

Now, a number of observations can be made based on above equation as follows:

(a) The dissipated energy is smaller than for the conventional case, if the charging time *T* is larger than *2RC*. That is, the dissipated energy can be made arbitrarily small by increasing the charging time.

(b) Also, the dissipated energy is proportional to *R*, as opposed to the conventional case, where the dissipation depends on the capacitance and the voltage swing. Thus, reducing the on-resistance of the PMOS network will reduce the energy dissipation.

III. Implementation of adiabatic logic circuits

Practical adiabatic families can be classified as either partially adiabatic IC or fully adiabatic. In Partially adiabatic circuits, some charge is allowed to be transferred to the ground, while in a fully adiabatic circuits, all the charge on the load capacitance is recovered by the power supply. Fully adiabatic circuits face a lot of problems with respect to the operating speed and the inputs power clock synchronization. Partially Adiabatic families include the following: Efficient Charge Recovery Logic (ECRL), Improved Efficient Charge Recovery Logic (IECRL), 2N-2N2P Adiabatic Logic, Positive Feedback Adiabatic Logic (PFAL), NMOS Energy Recovery Logic (NERL), Clocked Adiabatic Logic (CAL), True Single-Phase Adiabatic Logic (TSEL), and Source-coupled Adiabatic Logic (SCAL).

Some Fully adiabatic logic families include: Pass transistor Adiabatic Logic (PAL). Split-Rail Charge Recovery Logic (SCRL). Adiabatic logic achieves low power by maintaining small potential differences across the transistors while they are conducting, and allowing the charge stored in the output load capacitors to be recycled. A power-clock supply plays an important role in adiabatic switching. When it ramps up or down steadily, the power-clock supply causes a very small drop across the switching device. The power-clock supply not only supplies the energy but also recovers it. Adiabatic inverters are the simplest form of benchmark circuit to demonstrate the principle of energy recovery and the adiabatic principle. Our experiments on adiabatic inverters show that the energy recovery can be up to 80% if the transistors are minimally sized. The adiabaticity is observed up to a frequency governed by the circuit time-constant

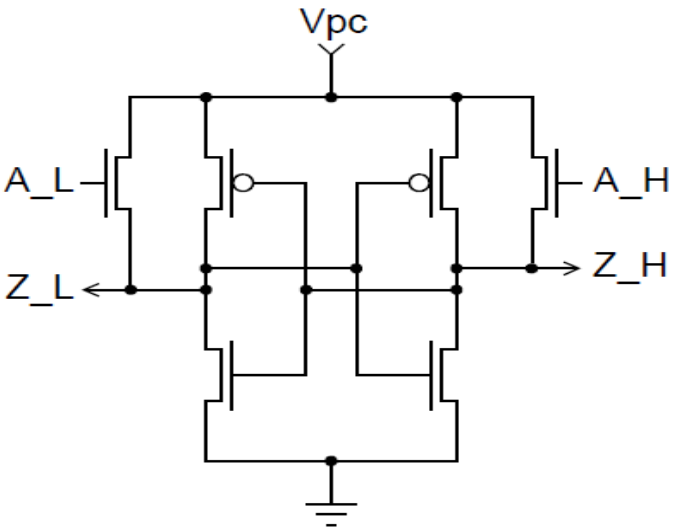

Fig2 Positive Feedback Adiabatic Logic (PFAL)

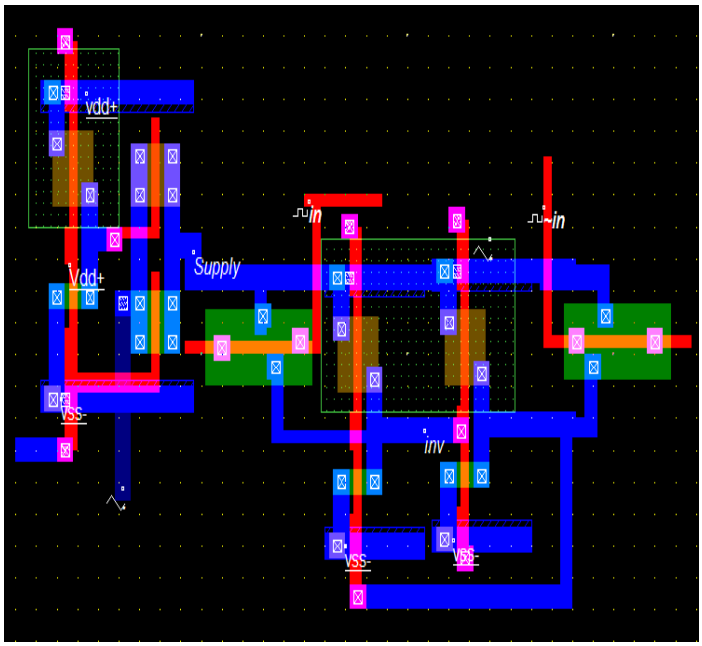

Fig3 Positive Feedback Adiabatic Logic (PFAL)

PEAL is based on a pair of cross-coupled inverters, with NMOS devices are connected between the outputs and the power-clock can allow complete recovery of those outputs.

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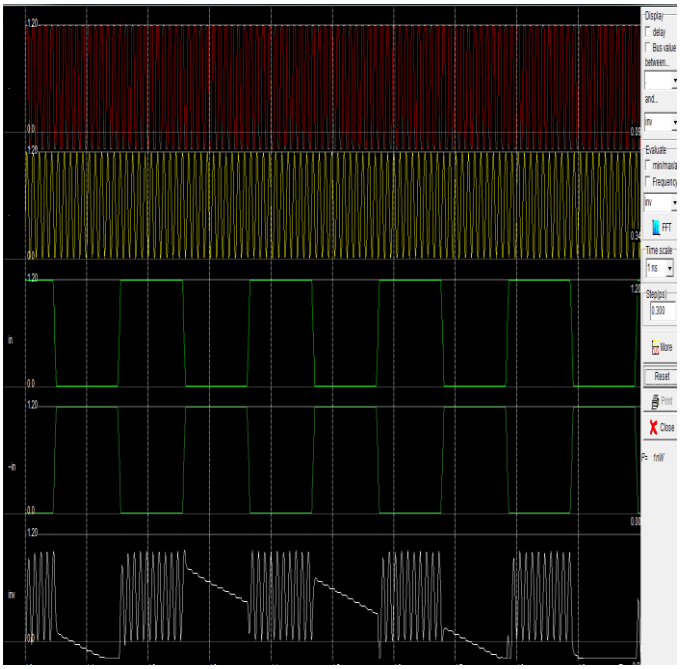

Fig4 Positive Feedback Adiabatic Logic (PFAL) with power supply

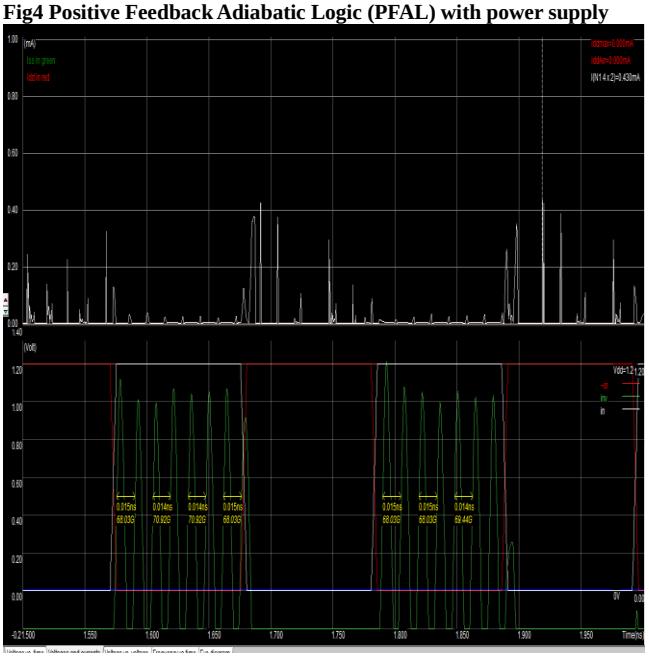

Fig5 Positive Feedback Adiabatic Logic (PFAL)

In order to recover and to reuse the supplied energy, an ac power supply is used for ECRL gates. As usual in adiabatic circuits, the supply voltage also acts as clock. Both out and out are generated so that the power clock generator can always drive a constant load capacitance, independent of the input signal. If the circuit operates correctly, energy has an oscillatory behavior, because a large part of the energy supplied to the circuit is given back to the power supply. As usual for adiabatic logic the energy behavior follows the supply voltage. In the same figure we may observe that, due to a coupling effect, the low level output goes to a negative voltage value during the recovery phase (that is, when the supply voltage ramps down). We define "Dissipated Energy" as the difference between the energy that the circuit needs to load the output capacitance, and the energy that the circuit gives back to the power supply during the recovery phase. The dissipated energy value depends on the input sequence and on the switching activity factor therefore the dissipated energy per cycle can be obtained from the mean value of the whole sequence. It can also be seen that a larger energy is dissipated if the input state changes and therefore the output capacitances have to switch.

	Static CMOS	IECRL	PFAL	Adia INV	With power	multiplier
No of MOSFET		5NMOS 2PMOS	4NMOS 2PMOS	3NMOS 2PMOS	6NMOS 4PMOS	58NMOS 58PMOS
Rise delay		16ns	0.02ns	0.02ns	0.02ns	0.02ns
Fall delay		9ns	0.03ns	0.03ns	0.03ns	0.03ns
Freq at Vdd	1.125 GHz	9.132 GHz	68 GHz	45 GHz		
Power dissipation	3 µW	15 µW	15 µW	1 µW	1 µW	1 µW
Maxm drain current	0.16 mA	0.20 mA	0.26mA	0.20 mA	0.20 mA	0.20 mA
Power efficiency		65	65	72	95	95
Threshold vtg		0.4V	0.4V	0.4V	0.4V	0.4V

Table 1 Comparison table for parametric analysis of different adiabatic logics.

IV. Conclusion

The Energy dissipation in conventional CMOS circuits can be minimized through adiabatic technique. By adiabatic technique dissipation in PMOS network can be minimized and some of energy stored at load capacitance can be recycled instead of dissipated as heat. But the adiabatic technique is highly dependent on parameter variation. With the help of micro wind layout simulator, the energy consumption is analyzed by variation of parameter. In analysis PFAL (Positive Feedback Adiabatic Logic) are compared with conventional CMOS logic for inverter circuits. It is finding that adiabatic technique is good choice for low power application in specified frequency range. Power reduction is achieved by recovering the energy in the recovery phase of the supply clock. If input changes from zero to Vdd, the voltage drops abruptly across the load capacitor and ground through NMOS. Adiabatic logic achieves low power by maintaining small potential differences across the transistors while they are conducting, and allowing the charge stored in the output load capacitors to be recycled. A power-clock supply plays an important role in adiabatic switching. When it ramps up or down steadily, the power-clock supply causes a very small drop across the switching device. The power-clock supply not only supplies the energy but also recovers it. Adiabatic inverters are the simplest form of benchmark circuit to demonstrate the principle of energy recovery and the adiabatic principle.

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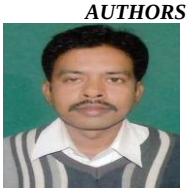

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